REMARKS

As pointed out above, the Invention I, claims 1-36 are elected for initial prosecution on the merits herein.

The TITLE is amended herein to more accurately describe the invention in light of the Restriction requirement issued by the Examiner.

The amendment to claims 1-5, 9, 13, 15, 18, 19, and 23-26 are not meant to further limit the scope of the claims. Rather, the changes are provided for clarity purposes.

The applicant respectfully submits that the pending claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN & SCHAEFF, LLP

By _____
Thomas E. Lees
Registration No. 46,867

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
(937) 223-2050
Facsimile: (937) 223-0724
E-mail: leest@kghs.com

Appendix A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A memory cell ~~having a square feature size of less than $4F^2$~~ comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel; and

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the square feature size of the memory cell is not greater than $2F^2$.

2. (Amended) The memory cell of claim 1, wherein the source ~~is~~ comprises a buried layer.

3. (Amended) The memory cell of claim 1, wherein the horizontal floating gate ~~is~~ comprises a sub lithographic floating gate.

4. (Amended) The memory cell of claim 1, wherein the horizontal floating gate ~~is~~ comprises a sub lithographic floating gate defined by a spacer.

5. (Amended) The memory cell of claim 1, wherein the horizontal floating gate ~~is~~ comprises a self aligned floating gate.

9. (Amended) The memory cell of claim 6, wherein the memory cell has a square feature size not greater than $2F^2$.

13. (Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a first n-type layer;

a p-type layer formed over the first n-type layer; and

a second n-type layer ~~is~~ formed over the p-type layer, wherein the p-type layer forms a substantially vertical channel, wherein the memory device has memory cells having feature size of less than $4F^2$.

15. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a h rizontal first n-type layer formed over a substrate;

a p-type layer formed over the first n-type layer;

a horizontal second n-type layer ~~is~~ formed over the p-type layer;

a horizontal floating gate formed over the substrate; and

a vertical select gate formed over the substrate, wherein the p-type layer forms a vertical channel, the first n-type layer forms a buried source and the second n-type layer forms a drain.

18. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

~~A~~ a buried source formed over a substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel, wherein the vertical channel is formed using epitaxial deposition.

19. (Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a buried source formed over a substrate;

a vertical channel formed over the buried source;

a drain formed over the vertical channel;

a floating gate formed over the substrate; and

a select gate formed perpendicular to the floating gate in a trench formed in the substrate, wherein the memory device has a square feature size of less than $4F^2$.

23. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench ~~is~~ formed in the substrate;

a vertical select gate ~~is~~ formed in the select trench;

digitlines are formed over the second n-type layer;

a self aligned floating gate formed over the n-type layer; and

wordlines formed over the substrate and the digitlines.

24. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench ~~is~~ formed in the substrate;

a vertical select gate ~~is~~ formed in the select trench;

a conductive layer ~~is~~ formed over at least a portion of the second n-type layer;

a first spacer ~~is~~ formed on the conductive~~tungsten~~ layer;

a tunnel oxide layer formed over at least a portion of the substrate;

a polysilicon layer formed on the tunnel oxide layer; and

an oxide layer formed on the polysilicon layer.

25. (Amended) The memory device of claim 24, wherein the conductive layer ~~is~~ comprises a tungsten layer.

26. (Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a first n-type layer formed over a substrate~~,~~ forming a source;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer~~,~~ forming a drain;

a select trench ~~is~~ formed in the substrate;

a select gate ~~is~~ formed substantially vertical in the select trench, wherein the memory device has a feature size substantially less than $4.5F^2$ ~~or not greater than $2F^2$~~.